

Achievable Throughput Optimization in OFDM Systems in the Presence of Interference and its Application to Power Line Networks

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Abstract

The aim of this paper is to study the bit-loading and power allocation problem in the presence of interference (Inter-carrier Interference (ICI) and Inter-Symbol Interference (ISI)) in Orthogonal Frequency Division Multiplexing (OFDM) systems. ISI and ICI significantly degrade the performance of OFDM systems and make the resource management optimized without the assumption of interference less efficient. To solve this problem, an initial solution based on the greedy approach is proposed in this paper. Then, several reduced complexity approaches, which yield a little degradation compared to the initial solution, have been developed. Simulation results presented in the context of Power Line Communication (PLC) show that the performance of proposed algorithms is tight with their upper bound. Moreover, these algorithms efficiently improve the system performance as compared to the constant power water-filling allocation algorithm as well as maximum power allocation algorithm.

Index Terms

Bit-loading, Power allocation, ICI, ISI, Power Line Communication, Windowed-OFDM, Greedy Algorithm.

I. INTRODUCTION

In the past decades, the use of PLC systems for high rate indoor broadband communications has spread rapidly. No-new-wire makes the PLC economically attractive for indoor LAN and become a complementary technology to wireless technologies such as WLAN [1], [2].

PLC systems exploit the OFDM technique to combat the effect of multi-path channels with severe frequency selectivity [3], [4]. The conventional OFDM divides the entire bandwidth into

many orthogonal subcarriers and data are transmitted in parallel over these subcarriers. Therefore, it can support high transmission data rate and achieves high spectral efficiency. Unfortunately, many phenomena such as frequency offset between transmitter and receiver, insufficient guard interval or Doppler frequency shift, etc. induce inter-carrier interference (ICI) as well as inter-symbol interference (ISI) that significantly degrade the performance of OFDM systems [5], [6] and make the resource management more complicated. Many techniques have been developed to combat the effects of ISI and ICI, such as time domain windowing [7], frequency-domain equalization [8] or ISI and ICI self-cancellation [9].

Both current and next generation of PLC systems employ frequency band from 2 to 30 MHz (and over), e.g., HPAV1, HPAV2, IEEE P1901, ITU-T G.9963 [2], [10]. In this frequency band, many radio applications such as amateur radio, urgency and military services have already been exploited. To avoid interference with those systems, a spectral mask is specified for PLC systems [10]. The IEEE P1901 standard uses the Windowed-OFDM instead of the conventional OFDM technique to adapt to the spectral mask [10]. In [11], the HS-OQAM is proposed for future use to increase the data rate as well as adapt to new spectral masks in Europe.

Regarding resource allocation, the bit-loading can be designed to achieve different objectives in OFDM systems, such as bit allocation, power allocation, code rate adaptation, etc. Different algorithms have been proposed among which we can enumerate: adaptive-rate algorithms which maximize the capacity under the power and bit-error rate constraints (BER) [12], [13]; margin-adaptive algorithms which minimize the consumed power under data rate and BER constraints [14]; BER minimization under data rate and power constraints [15]. If the ISI and ICI are present, the system can be modeled as a Gaussian interference channel [16]. In this case, by using joint coding and decoding, the system capacity is maximized by using the water-filling algorithm derived in [16]. In the absence of joint coding and decoding, the interference is considered as noise when solving the resource allocation problem [17], [18], [19], [20], [21]. In [18], the achievable throughput of PLC systems is maximized by combining the bit-loading algorithm and adaptive cyclic prefix. The bit-loading algorithm used in [18] relies on two simplifying assumptions. First, the conventional OFDM is taken into account to calculate ISI and ICI in PLC systems while, as mentioned above, PLC systems exploit the Windowed-OFDM instead of the conventional OFDM. The second simplification is enabled by on/off power loading and integer bit number constraint. The latter leads to bit discretization that causes non optimal power

use. Actually, the discretized bit-loading can be achieved with lower power consumption than with the approach in [18] and the residual power could be exploited to increase data rate or/and transmission quality. CP design for maximizing the achievable throughput for Windowed-OFDM systems is considered in [22]. Unfortunately, the power allocation strategy in [22] is also non optimal due to the bit discretization. In [18], [22], it is shown that the choice of a cyclic prefix (CP) length equal to the channel impulse response length makes PLC systems less efficient in terms of achievable throughput. Shorter CP evidently results in ISI and ICI, but the gain offered by shortened CP may exceed the losses caused by interference. Another approach to CP length adaptation relies on the statistical channel state information as derived in [23], [24]. This approach causes a capacity loss when compared to the bit and power allocation with the instantaneous channel state information (CSI). In our paper, we assume that perfect instantaneous CSI is available and we use it to optimize the resource allocation. Moreover, our interest is to optimize the throughput for fixed GI length and we take into account possible interference in the bit/power allocation.

Recently, several approaches to search for the upper-bound of the achievable throughput have been studied in [19] but no practical solution of the achievable throughput maximization problem with low-complexity has been given. A solution based on the greedy approach has been developed in [25] for the multi-carrier interference channel in multi-users ADSL systems. However, it only takes into account the ICI caused by the asynchronous cross-talk effect. Moreover, due to the difficulty of exact additional power computation, the algorithm in [25] exploits the gradient information to approximate the power adjustment when modifying the number of bits on subcarriers. The algorithm detailed in [25] approximates the matrix inversion via power series expansion to reduce the complexity. This method works only if the assumption of convergence of the power series expansion is valid. In this paper, we focus on single-user Windowed-OFDM-based systems in the presence of ICI as well as ISI. Our proposed algorithms are also based on the greedy principle, which is detailed in the section III. However, a judicious iterative procedure for accurate matrix inversion calculation and an iterative bit-loading procedure exploiting the incremental power needed to transmit an additional bit are utilized instead of the approximations proposed in [25].

The main contribution of this paper is to use the greedy principle to solve the achievable throughput maximization problem in PLC systems in the presence of interference and under

power and bit-error rate constraints. For this purpose, the ISI and ICI due to the presence of insufficient cyclic prefix in PLC systems have been analyzed. Relying on the ISI and ICI analysis and the greedy principle, we propose an initial greedy algorithm to calculate the achievable throughput maximization in the presence of ISI and ICI. Then, several approaches are proposed in order to reduce the complexity with a negligible degradation compared to the initial greedy solution.

The rest of the paper is organized as follows. In Section II, the OFDM model in the presence of ISI and ICI is described. In Section III, the greedy principle and several approaches to reduce the complexity are presented. In Section IV, the achievable throughput maximization problem is formulated and an initial solution, which exploits the greedy principle is given. A reduced complexity algorithm is also proposed. Numerical results are reported in Section V. Finally, conclusions and perspectives are drawn in Section VI.

II. SYSTEM MODEL

Let us consider a Windowed-OFDM system with L subcarriers used out of M , which are activated under a given spectral mask constraint. The demodulated sample on the m_0 -th used subcarrier and n_0 -th OFDM symbol is given by

$$y(m_0, n_0) = \alpha(m_0, n_0)c_{m_0, n_0} + ICI(m_0, n_0) + ISI(m_0, n_0) + b(m_0, n_0), \quad (1)$$

where $\alpha(m_0, n_0)$, c_{m_0, n_0} , $ISI(m_0, n_0)$, $ICI(m_0, n_0)$, $b(m_0, n_0)$ denote the channel multiplicative factor, the symbol of interest, the ISI and ICI coefficients and the complex circularly Gaussian noise sample at the m_0 -th used subcarrier and n_0 -th OFDM symbol.

We assume that the channel is block-based time invariant. Without loss of generality and for the sake of simplicity, in a block of many OFDM symbols, Eq. (1) can be re-written as

$$y(m_0) = \alpha(m_0)c_{m_0} + ICI(m_0) + ISI(m_0) + b(m_0) \quad (2)$$

Since the number of subcarriers used in practical PLC systems is quite large, we assume that the interference on a given subcarrier is normally distributed (following the central limit theorem) [3], [26]. Different normality tests for the interference have been introduced in [3]. These tests have confirmed the validity of gaussian distribution of the interference in practical PLC systems.

Then, the signal to interference plus noise ratio (SINR) and the theoretical capacity on the m_0 -th used subcarrier are given as follows:

$$SINR(m_0) = \frac{|\alpha(m_0)|^2 P(m_0)}{P_{ICI}(m_0) + P_{ISI}(m_0) + \sigma_b^2(m_0)} \quad (3)$$

$$C(m_0) = \log_2 \left(1 + \frac{SINR(m_0)}{\Gamma} \right) \quad (4)$$

where $P(m_0)$ is the power allocated to m_0 -th used subcarrier and Γ is the SNR gap that models the practical modulation and coding scheme for a targeted symbol-error rate (SER):

$$\Gamma = \frac{1}{3} \left[Q^{-1} \left(\frac{SER}{4} \right) \right]^2 \quad (5)$$

where $Q^{-1}(x)$ is the inverse tail probability of the standard normalization distribution [27].

Let us denote A^{use} the set of used subcarriers, then $\#(A^{use}) = L$, where $\#$ denotes the cardinality of A^{use} . On a given subcarrier, the interference power generally depends on the power allocated to other used subcarriers (see Appendix) and can be written as

$$P_I(m_0) = P_{ICI}(m_0) + P_{ISI}(m_0) = \sum_{m=1}^L W(m_0, m) P(m) \quad (6)$$

where $W(m_0, m)$ is the interference contribution of the m -th used subcarrier on the m_0 -th used subcarrier. In other words, $W(m_0, m)$ is the interference contribution of the m -th entry of A^{use} on the m_0 -th entry of A^{use} .

Let \mathbf{W} denote the interference matrix with entry (a, b) equal to $W(a, b)$ for $a, b \in \{1, \dots, L\}$. Let \mathbf{P} denote the allocated power vector and \mathbf{N} the noise power vector. The total interference power and the SINR on the m_0 -th used subcarrier are given by

$$P_I(m_0) = [\mathbf{WP}](m_0) \quad (7)$$

$$SINR(m_0) = \frac{|\alpha(m_0)|^2 P(m_0)}{P_I(m_0) + N(m_0)} \quad (8)$$

III. GREEDY PRINCIPLE AND REDUCED COMPLEXITY APPROACHES

In this section, we present the greedy principle for the discrete bit-loading problem. Hereafter, only the active subcarriers are taken into account except in the Appendix.

A. Greedy principle to solve the bit-loading problem

Let \mathbf{B} , \mathcal{A} , \mathcal{Q} and \mathcal{C} denote the bit-allocation vector, the allowable set of numbers of bits that correspond to available modulations on subcarriers, the objective function and the set of constraints (power constraints, data rate constraints, BER constraints). As \mathcal{Q} and \mathcal{C} depend on \mathbf{B} , the corresponding optimization problem can be written as

$$\mathcal{Q}(\mathbf{B}); \mathbf{B} \in \mathcal{A}^L, \mathcal{C}(\mathbf{B}) \quad (9)$$

An algorithm is said to be greedy if every decision taken at any stage is the one with the most obvious immediate advantage. That is to say it makes a locally optimal choice in the hope that successive choices will lead to a globally optimal solution. Generally, a greedy algorithm does not produce a global optimum, but nonetheless it may yield a local optimum that approximate well a global optimum [28].

In practice, the standard greedy algorithm initializes vector $\mathbf{B} = \{b(m)\}_{m=1,\dots,L}$ to the null vector. Another way to initialize the bit-loading vector relies on the water-filling and the bit discretization. This approach has been exploited in [29]. In [29], it is shown that the use of this initialization in the interference-free systems can strongly reduce the complexity with a negligible throughput loss when compared to the standard greedy algorithm. Then, the greedy process successively increases the number of bits on the subcarriers up to its upper level in \mathcal{A} , according to a predefined cost function \mathcal{F} , which enables to optimize \mathcal{Q} . The cost function is practically defined according to the objective function and taking into account the constraints. For example, for the throughput maximization problem under the total power constraint, the cost function is defined as the required upgrade power [30], [31] or as the gradient information in [25] or as the metrics of log-likelihood ratios (LLRs) for the throughput maximization under the BER constraint [32]. Generally, the cost function values depend on the subcarrier index and the iteration. We denote by $\mathcal{F}(m, k)$ the cost function value associated to an increase of the number of bits on the m -th subcarrier at the k -th iteration. At the k -th iteration, the greedy principle evaluates $\mathcal{F}(m, k)$ for all values of m and decides which subcarrier will be allocated additional bits. The number of bits on the m_0 -th subcarrier, i.e. $b(m_0)$, is increased after k -th iteration if

$$\begin{cases} m_0 = \arg \min_m \mathcal{F}(m, k), & \forall m \in [1, L] \\ \mathcal{C}(\mathbf{B}) \end{cases} \quad (10)$$

From (10), even if $\mathcal{F}(m_0, k)$ is the minimum value of $\mathcal{F}(m, k)$, if there exists any unsatisfied constraint, then the number of bits allocated to the subcarrier cannot be increased. In this case, to avoid meaningless loops, the cost function $\mathcal{F}(m_0, k)$ is set to infinity and this subcarrier must not be considered for additional bits allocation in following iterations. The procedure stops if there is no subcarrier left to allocate additional bits.

B. Reduced complexity approaches

In many cases, although the use of the greedy principle described in Section III-A yields an efficient solution to the problem in Eq. (9), its high complexity makes it unfeasible in practice. Since the complexity depends on the computational effort to calculate the cost function and the number of iterations, it can be reduced in particular by using computationally less expensive approximation of the cost function. On the other hand, the number of iterations depends on the bit-loading vector initialization and the number of simultaneously increased subcarriers per iteration. Thus, the number of iterations can be reduced by choosing a judicious initial bit-loading vector instead of a null vector and by simultaneously processing several subcarriers per iteration. We will see that these modifications lead to reduced complexity approaches at the expense of a little degradation compared to the greedy solution. In the next sections, the greedy principle and the reduced complexity approaches are utilized to form a reduced complexity algorithm that closely solves the achievable throughput maximization problem in single-user Windowed-OFDM systems in the presence of ISI and ICI. In the simulation part, this algorithm is applied in the context of PLC systems.

IV. ACHIEVABLE THROUGHPUT OPTIMIZATION IN THE PRESENCE OF INTERFERENCE

The achievable throughput optimization problem is difficult when taking into account ISI and ICI. In fact, even with the continuous bit allocation relaxation, the rate-adaptive problem in the presence of ISI and ICI cannot be easily solved because the term $P(m)$, which is the power allocation on the m -th subcarrier, exists both in the numerator as well as in the denominator of the throughput calculation formula (see Eq. (3), (4)). In [31] the solutions for both continuous and discrete bit-loading in the presence of ICI are determined. Nevertheless, the proposed bit-adding algorithm with null initial bit-loading vector for the discrete bit-loading remains highly complex. In [17], the power allocation corresponding to the continuous bit-loading optimization

is derived. It indicates that the mutual in-out information is not a convex function of the input power distribution and that the optimal solution must be obtained via an exhaustive search that is equivalent to an NP-hard problem. In the simulation part, we give an illustration of the non-convexity of the mutual information.

Let \mathcal{A} be the allowable set of number of bits associated to allowable modulations specified by the standard and \mathcal{T}_d be the down discretization function defined as

$$\mathcal{T}_d (\mathcal{R}^+ \rightarrow \mathcal{A}) : x \rightarrow \max\{T \in \mathcal{A} : T \leq x\} \quad (11)$$

Then, the achievable throughput optimization problem under the power constraints in single-user Single Input Single Output (SISO)-OFDM systems can be expressed as (12). The second constraint in (12) is to satisfy a given spectral mask. Problem (12) closely resembles the multi-user power control problem in digital subscriber lines (DSL) systems. The multi-user power control can be solved by the optimal spectrum balancing (OSB) [33], [34] and the iterative spectrum balancing (ISB) [34], [35], which decompose the initial problem into smaller problems corresponding to each subcarrier.

$$\begin{cases} \max R = \sum_{m=1}^L \mathcal{T}_d \left(\log_2 \left(1 + \frac{P(m)|\alpha(m)|^2}{([\mathbf{WP}](m) + N(m))\Gamma} \right) \right) \\ \sum_{m=1}^L P(m) \leq P_{total} \\ 0 \leq P(m) \leq P_{max}(m), \quad \forall m \in [1, L] \end{cases} \quad (12)$$

The complexity of these algorithms depends on the number of subcarriers and their practical complexity gain is normally obtained with a significant number of subcarriers. In our case, the optimization problem is equivalent to the achievable throughput optimization problem for L users on a single subcarrier. Thus, those algorithms are not interesting for our problem, which is equivalent to a single subcarrier problem. In addition, calculating the global optimum is very complex and the problem is only solvable when it involves few variables [36], [37]. In the following, relying on the greedy principle described in Section III-A, greedy algorithms as well as a reduced complexity algorithm for the achievable throughput maximization problem in the presence of ISI and ICI are derived.

A. Bit number – Power level relation

Firstly, we do not consider any constraint on the power allocated on each subcarrier and we search the solution for the following problem: given $\mathbf{B} = [b(1), b(2), \dots, b(L)]^T$ the vector of number of bits allocated to subcarriers, we find the power vector $\mathbf{P} = [P(1), P(2), \dots, P(L)]^T$ so that:

$$\log_2 \left(1 + \frac{P(m)|\alpha(m)|^2}{([\mathbf{WP}](m) + N(m))\Gamma} \right) = b(m), \quad \forall m \in [1, L] \quad (13)$$

Let us note

$$\frac{P(m)}{[\mathbf{WP}](m) + N(m)} = \frac{(2^{b(m)} - 1)\Gamma}{|\alpha(m)|^2} = \lambda_m \quad (14)$$

Then, re-writting Eq. (14) in the matrix form, we obtain:

$$\begin{aligned} \mathbf{P} &= \Lambda_{(\mathbf{B})}\mathbf{WP} + \Lambda_{(\mathbf{B})}\mathbf{N} \\ \Rightarrow \mathbf{P} &= (\mathbf{I} - \Lambda_{(\mathbf{B})}\mathbf{W})^{-1}\Lambda_{(\mathbf{B})}\mathbf{N} \end{aligned} \quad (15)$$

where $\Lambda_{(\mathbf{B})} = \text{diag}(\lambda_1, \dots, \lambda_L)$. Equation (15) yields the solution of problem (13) alone without the constraints imposed on the power allocated to the subcarriers. However, power constraints always exist, i.e. $0 \leq P(m) \leq P_{\max}(m)$, then there are many cases where we can't find the power allocation corresponding to a given bit allocation and satisfying the set of constraints.

The monotonicity of the right-hand side of (15) has been already demonstrated in [25] where it is shown that if $\mathbf{B}_1 \leq \mathbf{B}_2$ component-wise, then the corresponding power vectors satisfy $\mathbf{P}_1 \leq \mathbf{P}_2$ component-wise. It means that when the number of bits on a subcarrier is increased, the resulting power levels on all subcarriers are higher than or equal to the current ones.

B. Greedy Algorithm

The standard greedy algorithm initializes $\mathbf{B} = 0$, that is to say $\Lambda = 0$ and $\mathbf{P} = 0$. Then it tries to successively increase the number of bits on the m -th subcarrier to its upper level according to the cost function \mathcal{F} and derives the allocated power by using (15). However, the difficulty of cost function construction causes the complicated implementation to this algorithm. The search for a relevant cost function for an optimal greedy algorithm is a complex problem because for every number of bits increase on any subcarrier, the power levels on all subcarriers must be changed to account for the increased interference. As mentioned above, both power constraints, i.e. total allocated power and spectral mask constraint, have to be taken into account to define the cost

function. In this paper, for the sake of simplicity, we only take into account the incremental power needed to transmit an additional bit as the cost function in our proposed solutions. This cost function has been utilized to solve efficiently the achievable throughput maximization problem in OFDM systems under the total power constraint [30], [31], [29]. The greedy-based algorithms such as the bit-adding (or bit-filling) and bit-subtracting (or bit-removal) are practically utilized to derive feasible solutions in many bit-loading optimization problems [32], [38], [39].

1) *Standard Algorithm:* Let us denote by \mathbf{P}_k the power allocation and by $\mathbf{\Lambda}_k$ the corresponding matrix (Eq. (14)) after iteration k . For an additional number of bits on the m -th subcarrier, $\mathbf{\Lambda}_{k+1}^{(m)}$ and $\mathbf{P}_{k+1}^{(m)}$ denote the new matrix and power allocation vector updated accordingly. Let $\text{tr}(\mathbf{A})$ denote the trace of vector \mathbf{A} . Then, the incremental power needed to transmit an additional bit on the m -th subcarrier at iteration $(k+1)$, is chosen as a cost function and defined by

$$\mathcal{F}(m, k+1) = \Delta P_{bit}(m, k+1) = \frac{\text{tr}(\mathbf{P}_{k+1}^{(m)} - \mathbf{P}_k)}{\Delta b_{k+1}^{(m)}} \quad (16)$$

The number of bits on the m_0 -th subcarrier is increased at iteration $(k+1)$ to its upper level in \mathcal{A} if

$$\begin{cases} m_0 = \arg \min_m \Delta P_{bit}(m, k+1) \\ \text{tr}(\mathbf{P}_{k+1}^{(m_0)}) \leq P_{total} \\ 0 \leq \mathbf{P}_{k+1}^{(m_0)}(m) \leq P_{max}(m), \quad \forall m \in [1, L] \end{cases} \quad (17)$$

After updating the number of bits on the m_0 -th subcarrier, $\mathbf{\Lambda}$ and \mathbf{P} become:

$$\mathbf{\Lambda}_{k+1} = \mathbf{\Lambda}_{k+1}^{(m_0)}; \quad \mathbf{P}_{k+1} = \mathbf{P}_{k+1}^{(m_0)} \quad (18)$$

As in Section III, the procedure is repeated until there is no subcarrier left to allocate additional bits.

The complexity of this standard algorithm is high. Let us denote by A_{on}^{k+1} the set of subcarriers to which we can allocate additional bits at iteration $(k+1)$ and $L_{on}^{k+1} = \#(A_{on}^{k+1}) (\leq L)$. At iteration $(k+1)$, L_{on}^{k+1} matrices of size $L \times L$ must be inverted to derive $\mathbf{P}_{k+1}^{(m)} \forall m \in A_{on}^{k+1}$. Hence, the complexity is about $\mathcal{O}(L^3 * L_{on}^{k+1})$ due to the matrix inversions for minimum search. This algorithm becomes intractable as the number of subcarriers becomes significant.

2) *Efficient computation of the cost function:* The complexity of the standard greedy algorithm is mainly due to matrix inversions in the cost function calculation. To reduce the complexity, an efficient method is proposed to solve the matrix inversion problem. From Eq. (15),

$$\mathbf{P}_k = (\mathbf{I} - \mathbf{\Lambda}_k \mathbf{W})^{-1} \mathbf{\Lambda}_k \mathbf{N} = \mathbf{M}_k \mathbf{\Lambda}_k \mathbf{N} \quad (19)$$

At the iteration $(k+1)$, if the bit allocation on the m -th subcarrier is increased by $\Delta b_{k+1}^{(m)}$, then

$$\Delta \lambda_{k+1}^{(m)} = \frac{(2^{b_k(m) + \Delta b_{k+1}^{(m)}} - 2^{b_k(m)}) \Gamma}{|\alpha(m)|^2} \quad (20)$$

$$\mathbf{\Lambda}_{k+1}^{(m)} = \mathbf{\Lambda}_k + \Delta \lambda_{k+1}^{(m)} \mathbf{e}_m \mathbf{e}_m^T \quad (21)$$

$$\mathbf{P}_{k+1}^{(m)} = (\mathbf{I} - \mathbf{\Lambda}_{k+1}^{(m)} \mathbf{W})^{-1} \mathbf{\Lambda}_{k+1}^{(m)} \mathbf{N} \quad (22)$$

where \mathbf{e}_m is a column vector that has m -th entry equal to 1 and the others equal to 0. Letting $\mathbf{M}_{k+1}^{(m)} = (\mathbf{I} - \mathbf{\Lambda}_{k+1}^{(m)} \mathbf{W})^{-1}$, we obtain:

$$\begin{aligned} \mathbf{M}_{k+1}^{(m)} &= (\mathbf{I} - \mathbf{\Lambda}_{k+1}^{(m)} \mathbf{W})^{-1} \\ &= (\mathbf{I} - \mathbf{\Lambda}_k \mathbf{W} - \Delta \lambda_{k+1}^{(m)} \underbrace{\mathbf{e}_m \mathbf{e}_m^T \mathbf{W}}_{\mathbf{W}_m})^{-1} \\ &= (\mathbf{M}_k^{-1} - \mathbf{e}_m \Delta \lambda_{k+1}^{(m)} \mathbf{W}_m)^{-1} \\ &= \mathbf{M}_k + \frac{\mathbf{M}_k \mathbf{e}_m \mathbf{W}_m \mathbf{M}_k}{\frac{1}{\Delta \lambda_{k+1}^{(m)}} - \mathbf{W}_m \mathbf{M}_k \mathbf{e}_m} \\ &= \mathbf{M}_k + \Delta \mathbf{M}_{k+1}^{(m)} \end{aligned} \quad (23)$$

$$\mathbf{P}_{k+1}^{(m)} = \mathbf{M}_{k+1}^{(m)} \mathbf{\Lambda}_{k+1}^{(m)} \mathbf{N} \quad (24)$$

Note that $\mathbf{M}_0 = \mathbf{I}$ because $\mathbf{B} = 0$ or equivalently $\mathbf{\Lambda}_0 = 0$ at the first iteration. At any iteration, we can derive the power vector $\mathbf{P}_{k+1}^{(m)}$ when the number of bits on m -th subcarrier is increased. We choose the m_0 -th subcarrier to increase its number of bits as in Eq. (17). Finally, matrix \mathbf{M} , the power vector and the bit-allocation corresponding matrix are updated to

$$\mathbf{M}_{k+1}, \mathbf{P}_{k+1}, \mathbf{\Lambda}_{k+1} = \mathbf{M}_{k+1}^{(m_0)}, \mathbf{P}_{k+1}^{(m_0)}, \mathbf{\Lambda}_{k+1}^{(m_0)} \quad (25)$$

Due to the simple expression of \mathbf{e}_m , the complexity of $\Delta \mathbf{M}_{k+1}^{(m)}$ calculation is only $\mathcal{O}(2L^2)$. Thus, the total complexity at iteration $(k+1)$ of this algorithm is $\mathcal{O}(4L^2 * L_{\text{on}}^{k+1})$, i.e. $\mathcal{O}(3L^2 * L_{\text{on}}^{k+1})$ to calculate $\mathbf{M}_{k+1}^{(m)}$, $\mathcal{O}(L^2 * L_{\text{on}}^{k+1})$ to calculate $\mathbf{P}_{k+1}^{(m)}$ for all the values of m . Finally, the complexity is reduced by a factor of about $L/4$ thanks to the proposed implementation of matrix inversion.

In the following, the greedy algorithm which uses this computation is called the proposed greedy algorithm and referred to as GR to distinguish from the standard greedy algorithm (Standard GR), which exploits the matrix inversion to calculate the cost function.

C. Reduced complexity approaches

In this section, we try to reduce the total complexity of the greedy algorithms by relying on the reduced complexity approaches proposed in Section III-B.

1) *Cost function approximation:* to further reduce total complexity, an approximation of the incremental power needed to transmit an additional bit on m -th subcarrier is proposed. By using Eq. (15), we obtain:

$$\begin{cases} \mathbf{P}_k - \Lambda_k \mathbf{W} \mathbf{P}_k &= \Lambda_k \mathbf{N} \\ \mathbf{P}_{k+1}^{(m)} - \Lambda_{k+1}^{(m)} \mathbf{W} \mathbf{P}_{k+1}^{(m)} &= \Lambda_{k+1}^{(m)} \mathbf{N} \end{cases} \quad (26)$$

Letting $\Delta \mathbf{P}_{k+1}^{(m)} = \mathbf{P}_{k+1}^{(m)} - \mathbf{P}_k$ and $\Delta \Lambda_{k+1}^{(m)} = \Delta \lambda_{k+1}^{(m)} \mathbf{e}_m \mathbf{e}_m^T$, the difference of equations in (26) yields

$$\Delta \mathbf{P}_{k+1}^{(m)} - \Lambda_k \mathbf{W} \Delta \mathbf{P}_{k+1}^{(m)} - \Delta \Lambda_{k+1}^{(m)} \mathbf{W} \mathbf{P}_k - \Delta \Lambda_{k+1}^{(m)} \mathbf{W} \Delta \mathbf{P}_{k+1}^{(m)} = \Delta \Lambda_{k+1}^{(m)} \mathbf{N} \quad (27)$$

We assume that $\Delta \Lambda_{k+1}^{(m)} \mathbf{W} \mathbf{P}_k \gg \Delta \Lambda_{k+1}^{(m)} \mathbf{W} \Delta \mathbf{P}_{k+1}^{(m)}$ or equivalently $[\mathbf{W} \mathbf{P}_k](m) \gg [\mathbf{W} \Delta \mathbf{P}_{k+1}^{(m)}](m)$, i.e. the interference increase on each subcarrier due to the increase of power allocation is negligible as compared to the current interference level on this subcarrier. This assumption is valid when the power allocation becomes high. In our simulations, it is valid with significant probability (>90%). Then, we can approximate $\Delta \mathbf{P}_{k+1}^{(m)}$ from Eq. (27) as

$$\Delta \mathbf{P}_{k+1}^{(m)} \approx (\mathbf{I} - \Lambda_k \mathbf{W})^{-1} \Delta \Lambda_{k+1}^{(m)} (\mathbf{W} \mathbf{P}_k + \mathbf{N}) \approx \mathbf{M}_k \Delta \lambda_{k+1}^{(m)} (\mathbf{W} \mathbf{P}_k + \mathbf{N}) \quad (28)$$

The required power per additional bit on m -th subcarrier is

$$\begin{aligned} \Delta P_{bit}(m, k+1) &= \frac{\text{tr}(\Delta \mathbf{P}_{k+1}^{(m)})}{\Delta b_{k+1}^{(m)}} \\ &\approx \frac{\text{tr}(\mathbf{M}_k(:, m)) \Delta \lambda_{k+1}^{(m)} [\mathbf{W} \mathbf{P}_k + \mathbf{N}](m)}{\Delta b_{k+1}^{(m)}} \end{aligned} \quad (29)$$

where $\mathbf{M}_k(:, m)$ is the m -th column vector of matrix \mathbf{M}_k . Note that the matrix inversion in the calculation of $\Delta P_{bit}(m, k+1)$ has already been calculated to derive \mathbf{P}_k :

$$\mathbf{P}_k = (\mathbf{I} - \Lambda_k \mathbf{W})^{-1} \Lambda_k \mathbf{N} = \mathbf{M}_k \Lambda_k \mathbf{N} \quad (30)$$

Then, at every iteration, the number of matrix inversions to calculate is only one. Thus the complexity reduction gain at iteration $(k + 1)$ is of about L_{on}^{k+1} as compared to the standard greedy algorithm.

2) *Reduction of the number of iterations:* The choice of null initial bit-allocation vector $\mathbf{B} = 0$ or equivalently $\mathbf{P} = 0$ and $\mathbf{\Lambda} = 0$ involved by the greedy approach makes the number of iterations high. We can enhance the convergence rate by judiciously initializing vector \mathbf{B} . An initial bit-loading vector that can be utilized is the bit-loading solution obtained by the water-filling followed by bit discretization. In other words, the power allocation obtained by the Constant Power Water-Filling (CPWF) [17] is used to calculate the continuous bit-loading. From the CPWF solution we perform the discrete bit-loading and we determine the corresponding power allocation applying (15). It is exploited to judiciously initialize bit-loading and power allocation vectors.

Theorem 1. *The power allocation corresponding to the bit-loading initialized by CPWF algorithm followed by bit discretization always satisfies the power constraints.*

Proof. Let \mathbf{C}_{CPWF} and \mathbf{P}_{CPWF} be the continuous bit-loading and power allocation vectors obtained by the CPWF algorithm; \mathbf{B}_0 and \mathbf{P}_0 be the discrete bit-loading vector and its corresponding power allocation vector after the discretization and from the monotonicity of the right-hand side of (15) (see VI.A), we obtain:

$$\mathbf{0} \leq \mathbf{B}_0 \leq \mathbf{C}_{CPWF} \Rightarrow \mathbf{0} \leq \mathbf{P}_0 \leq \mathbf{P}_{CPWF} \quad (31)$$

or equivalently,

$$\begin{cases} 0 \leq P_0(m) \leq P_{CPWF}(m) \leq P_{\max}(m), \forall m \\ \sum_{m=1}^L P_0(m) \leq \sum_{m=1}^L P_{CPWF}(m) = P_{\text{total}} \end{cases} \quad (32)$$

This demonstrates that \mathbf{P}_0 satisfies the power constraints. \square

In the simulations, it is shown that the performance obtained by choosing the initial bit-loading vector obtained by the water-filling and bit discretization is slightly different from the one obtained by choosing a null one. The proposed greedy algorithm combined with this initialization is referred to as GR + Init in the simulations.

For further complexity reduction, we tried to simultaneously increase the number of bits on K

subcarriers per iteration corresponding to the K minimum values of the cost function instead of only one subcarrier per iteration as in the previous approaches. At any iteration, if the number of bits on K subcarriers cannot be increased simultaneously, then we try to increase them one by one.

3) *Proposed reduced complexity algorithm:* Applying the above reduced complexity approaches results in a reduced complexity algorithm (RCA). The initial discrete bit-loading vector obtained by the CPWF followed by bit discretization algorithm, the cost function approximation and the simultaneous increase of K subcarriers per iteration are utilized in this proposed algorithm. The average complexity per iteration is dominated by matrix inversion computation.

Let $\bar{L}_{on} = \beta L$, ($0 < \beta < 1$) be the average number of subcarriers that can be allocated additional bits at each iteration, i.e. $\bar{L}_{on} = \frac{1}{N} \sum_{k=0}^{N-1} L_{on}^k$, where N is the number of iterations. To illustrate the total complexity, the equivalent number of matrix inversions is calculated by normalizing the total complexity with the complexity of inversion matrix (the complexity of a matrix inversion is $\mathcal{O}(L^3)$). The complexity per iteration, the number of iterations and the equivalent total number of matrix inversions are shown in Table 1 where $\beta_1 < \beta$.

Algorithm	Complexity per iteration	Number of iterations	Number of matrix inversions
Standard GR	$\approx \mathcal{O}(\beta L^4)$	N_s	$N_s * \mathcal{O}(\beta L)$
GR	$\approx \mathcal{O}(4\beta L^3)$	N_s	$N_s * \mathcal{O}(4\beta)$
GR + Init	$\approx \mathcal{O}(4\beta_1 L^3)$	$N_1 < N_s$	$N_1 * \mathcal{O}(4\beta_1)$
RCA	$\approx \mathcal{O}(L^3)$	$N_K < N_s$	$N_K * \mathcal{O}(1)$

Table 1. Complexity per iteration, number of iterations and equivalent total number of matrix inversions.

D. The convergence of the algorithms

All algorithms studied in this paper always converge. The proof of this convergence relies on the monotonicity of the right-hand side of (15) and bit number increment in the Greedy process. The initial power allocation vector always satisfies the power constraints. At every iteration, we try to increase the number of bits on the subcarriers or equivalently, to setup a new bit-loading

vector that is greater (component wise) when compared to the current bit-loading vector. This leads to the increase of power allocation vector. However, the constrained area of the power allocation vector is bounded. Hence, all proposed algorithms converge to a final state, which depends on the initial bit-loading vector and the way the subcarriers are chosen at every iteration.

V. SIMULATIONS RESULTS

The simulation parameters are given as follows:

- Single-user SISO-PLC system with the IEEE P1901 standard.
- $T_s = 0.01$ (μs), $T_0 = 40.96$ (μs) (IEEE P1901 standard).
- $GI = 5.56$ (μs), $RI = 4.96$ (μs) (IEEE P1901 standard).
- $\mathcal{A} = \{0, 1, 2, 3, 4, 6, 8, 10, 12\}$.
- $P_{max}(m) = 1$ (normalized to the spectral mask at $P_{mask} = -55$ dBm/Hz), $\forall m \in [1, L]$.
- $\Gamma = 4.038$, corresponding to $SER = 10^{-3}$.
- The channel impulse response (CIR) $h(t)$ is obtained by the IFFT of the frequency response of Tonello model (class 2) [40] and time rectangular filtering, keeping 95% of the initial energy [41].
- Noise model: Background noise (Esmailian model) [42].
- Number of channel realizations for Monte-Carlo simulation: 1000.

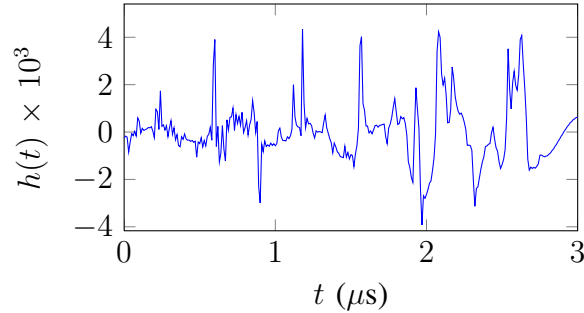


Fig. 1: An example of truncated CIR for Class 2 channel.

Figure 1 gives an example of CIR for Class 2 of Tonello model. The calculation of the interference power (i.e. the entries of matrix \mathbf{W}) in the case of insufficient guard interval (GI) in PLC systems is given in the Appendix. This calculation is different from the one derived in [43] for conventional OFDM systems. The first results of interference calculation for PLC systems were

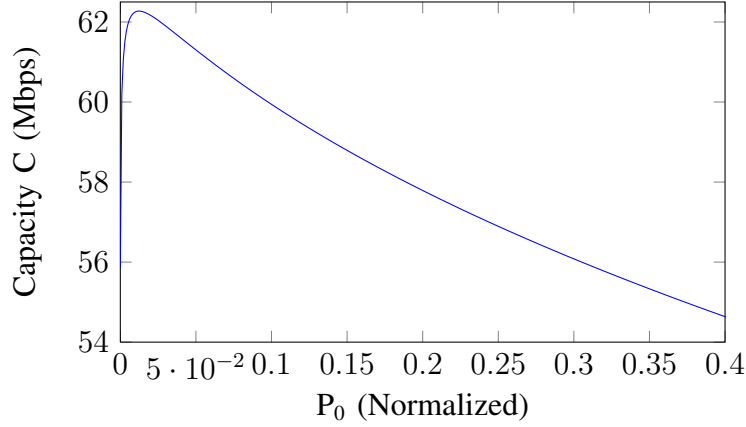


Fig. 2: An illustration of non-convexity of the problem (33).

presented in [11], [22]. In this paper, we present a more detailed calculation with both filters at the transmitter and at the receiver specified in the IEEE P1901 standard to obtain the analytical expression of the interference power and then calculate the entries of matrix \mathbf{W} .

A. Non-convexity of the problem

In this subsection, we illustrate the non-convex structure of the problem under study. The continuous version of the bit-loading problem (12) is stated as

$$\begin{cases} \max C = \sum_{m=1}^L \log_2 \left(1 + \frac{P(m)|\alpha(m)|^2}{([\mathbf{W}\mathbf{P}](m) + N(m))\Gamma} \right) \\ \sum_{m=1}^L P(m) \leq P_{total} \\ 0 \leq P(m) \leq P_{max}(m), \quad \forall m \in [1, L] \end{cases} \quad (33)$$

The non-convexity of the problem (33) has already been mentioned in [17]. To support this result, it is quite easy to find directions in the constrained power area where non-concavity arises. For instance, letting:

$$P(m) = \begin{cases} P_0 & m \in [401, 420] \\ 10^{-3} & m \in [1, 400] \cap [421, 917] \end{cases} \quad (34)$$

where P_0 linearly varies in from 0 to 0.4 (normalized to P_{mask}) yields non-concavity shape of C as in Fig. 2.

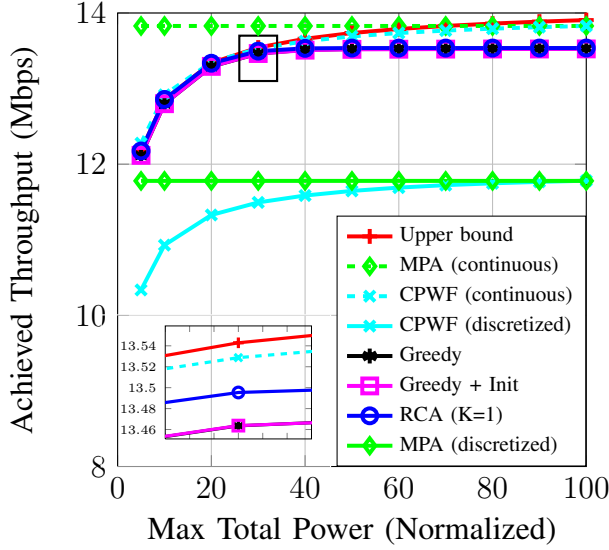


Fig. 3: Throughput of difference algorithms.

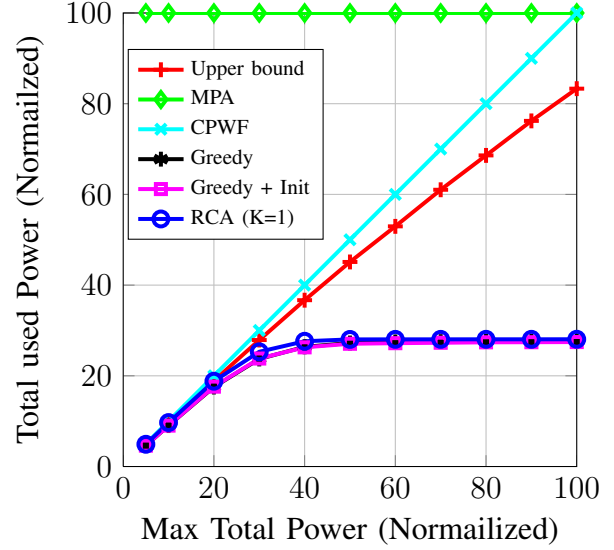


Fig. 4: Consumed power of algorithms.

B. Simulations restricted to a reduced subcarriers subset

For the sake of simulation run-time, in the first time, we only consider the first hundred subcarriers ($L = 100$) in the simulations. Moreover, we take the minimum allowable value of GI ($5.56 \mu s$) defined in the IEEE P1901 standard. In this case, the effect of interference on the system performance is significant. Figures 3 and 4 illustrate the achievable throughput and total consumed power for the proposed greedy algorithm (GR), the proposed greedy algorithm with the initialization with CPWF (GR + Init), the reduced complexity algorithm (RCA) with $K = 1$, the CPWF algorithm before/after discretization and throughput obtained with the maximum power allocation (MPA), which allocates the maximum allowable powers to the subcarriers, i.e. $P(m) = P_{max}(m)$, $\forall m$. Moreover, the upper bound of achievable throughput is also plotted. This upper bound is obtained by omitting the constraints of spectral mask, i.e. $P(m) \leq P_{max}(m)$, $\forall m$ in the problem (12). The efficient solution for the relaxed problem is given by the proposed greedy algorithm with the use of incremental power needed to transmit an additional bit as the cost function. The performance of GR and GR + Init algorithms in terms of achievable throughput is almost the same. The achievable throughput of the proposed RCA with $K = 1$ is little higher than that obtained with the GR algorithms and significantly improved as compared to the CPWF or MPA algorithm. For example, if the total exploitable normalized power is 50, the RCA with

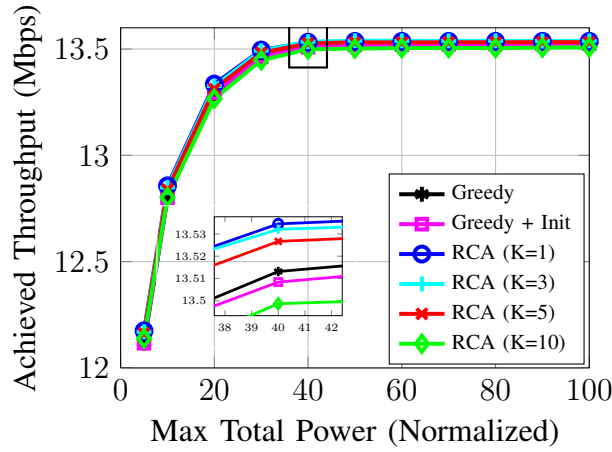


Fig. 5: Achievable throughput comparison.

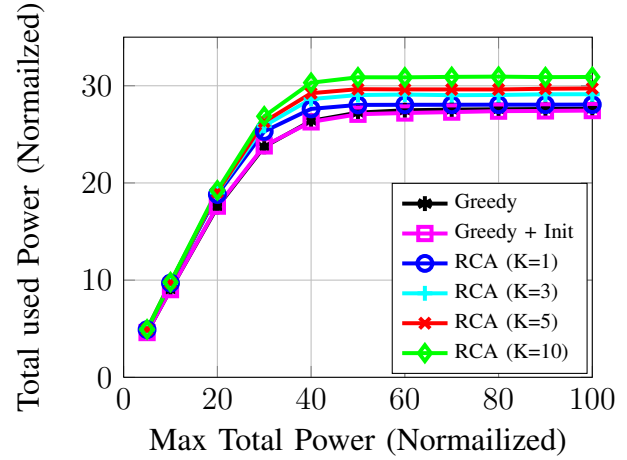


Fig. 6: Total consumed power comparison.

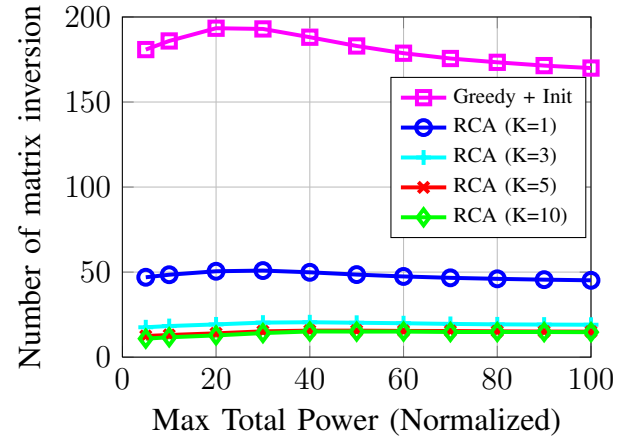
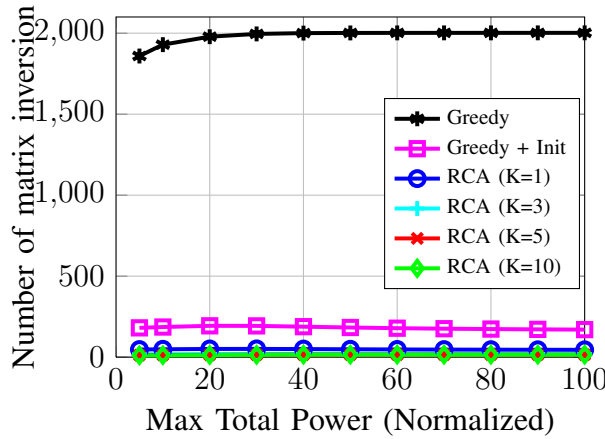


Fig. 7: Algorithms complexity comparison (1). Fig. 8: Algorithms complexity comparison (2).

$K = 1$ increases the throughput by 1% as compared to the GR algorithms and it outperforms by 16% (resp. 15%) the CPWF (resp. MPA) algorithm. Moreover, it reduces by 44% (resp. 72%) the total consumed power when compared to the CPWF (resp. MPA) algorithm.

Figures 5 and 6 show the comparison between the GR algorithms and the RCA with different values for K . It demonstrates that the achievable throughput of the RCA is slightly different as compared to that of the GR algorithm. The difference of achievable throughput between the GR algorithm and RCA is negligible ($<1\%$) and thus the RCA can be exploited to calculate the achievable throughput instead of the GR algorithm. The achievable throughput is decreased and

the total consumed power is increased when K is increased. It means that the use of power is less efficient when we increase K . In the case of the RCA with $K = 10$, the achievable throughput decreases by 0.3% while the computation cost is reduced by 99% (resp. 90%) (see Figure 7) when compared to the GR algorithm with null initial vector (resp. with initial vector obtained by CPWF). Note that this algorithm complexity is already strongly reduced as compared with the standard greedy algorithm that exploits the matrix inversion.

Finally, in Figures 7 and 8, we have plotted the complexity of the different algorithms. Figure 7 shows the complexity comparison between the GR algorithms and the RCA. We can see that the initialization with CPWF algorithm reduces significantly the complexity of the GR algorithm. The RCA has reduced the complexity by $>90\%$ (resp. 80%) as compared to the GR algorithm with null initial vector (resp. GR + Init). It is also seen that the complexity of RCA is decreased when K increases, which can be explained by the diminution of the number of iterations. Nevertheless, the complexity of both cases $K = 5$ and $K = 10$ is almost the same. This is due to the number of failed attempts. Remember that in the reduced complexity algorithm with $K > 1$, at every iteration, we try to simultaneously increase the number of bits on K subcarriers. However, at any iteration, if the attempt has failed, we must try to increase those K subcarriers one by one. This increases the number of matrix inversions.

Algorithm	Time per iteration (ms)	Number of iteration	Total time (ms)
Standard GR	110	517	56870
GR	28.1	517	14528
GR + Init	14.6	45	657
RCA ($K = 1$)	2	45	90
RCA ($K = 5$)	1.9	15	29
RCA ($K = 10$)	1.75	15	26.25

Table 2. Run-time per iteration, number of iterations and total run-time.

Table 2 lists the run-time per iteration, number of iterations and total run-time for the standard greedy, proposed greedy and reduced complexity algorithms. Those values are obtained in the case of $P_{total} = 90$ and with a computer equipped with a duo-core processor (2x2.7 GHz), RAM 4Gb and Matlab 2009. In this table, the GR algorithm reduces the total run-time by a factor

of 3.8 as compared to the standard greedy algorithm. This gain is almost the same as the run-time ratio between the direct inversion matrix calculation and the use of iterative calculation to calculate matrix inversion in Matlab. Indeed, the use of the initial bit-loading vector obtained by the CPWF algorithm reduces strongly not only the number of iterations but also the run-time per iteration due to the decrease of the average number of subcarriers for which we have to calculate the value of cost function. Table 2 also shows that the run-time per iteration of the reduced complexity algorithm and its number of iterations are much smaller when compared to the standard and proposed greedy algorithms. Hence, its total run-time is significantly reduced as compared to the standard and proposed greedy algorithms.

C. Simulation for a realistic PLC system

In this section, the proposed algorithm is applied to a realistic PLC system, where 917 subcarriers are considered ($L = 917$). The number of channel realizations is set to 200. Figures 9, 10 and 11 show the performance of RCA algorithms with $K = 5$ and $K = 20$ when compared to the CPWF algorithm followed by bit discretization for different classes of channel (class 2, 5 and 9) with a GI of $5.56 \mu s$. In these figures, the throughput obtained with RCA is increased by 17% (resp. 13%) as compared to that of CPWF algorithm for class 2 (resp. class 5) channel. In these cases, the interference is significant. However, for class 9 channel, the use of the CPWF and bit discretization is sufficient for an efficient bit-loading and power allocation because there is almost no interference or the interference power is insignificant as compared to the noise power. Moreover, in this case, all subcarriers have reached their maximum number of bits determined by the maximum constellation and the maximum power constraint. Thus, no additional iteration is required.

Moreover, the performance of RCA for different mandatory GI values from $5.56 \mu s$ to $47.12 \mu s$ (specified in the IEEE P1901 standard: 5.56, 7.56, 9.56, 11.56, 15.56, 19.56 and $47.12 \mu s$) is illustrated in Figure 12 with class 2 channel and $P_{total} = 500$ (normalized). In this figure, the RCA algorithms improve the achievable throughput by about 10% when compared to the CPWF + discretization. Moreover, we can observe that the GI value that maximizes the throughput coincides with the one that maximizes the capacity. This observation can be used to optimize jointly the GI value and bit/power allocation. In other words, firstly, we could use the CPWF algorithm to calculate the capacity for every value of GI specified in the IEEE P1901 standard.

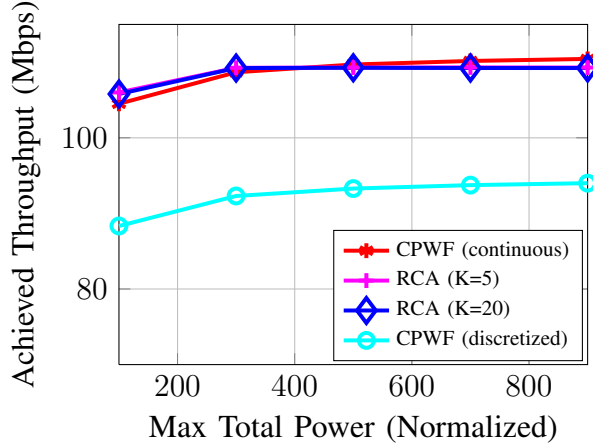


Fig. 9: RCA vs CPWF in Class 2 channel.

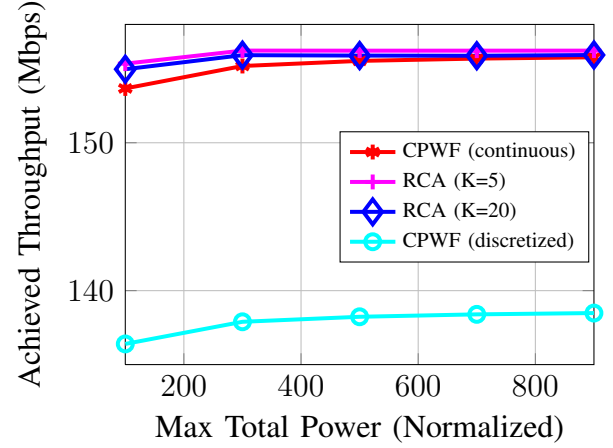


Fig. 10: RCA vs CPWF in Class 5 channel.

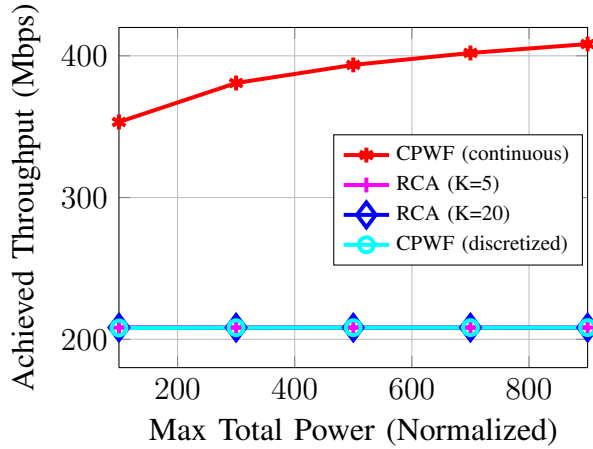


Fig. 11: RCA vs CPWF in Class 9 channel.

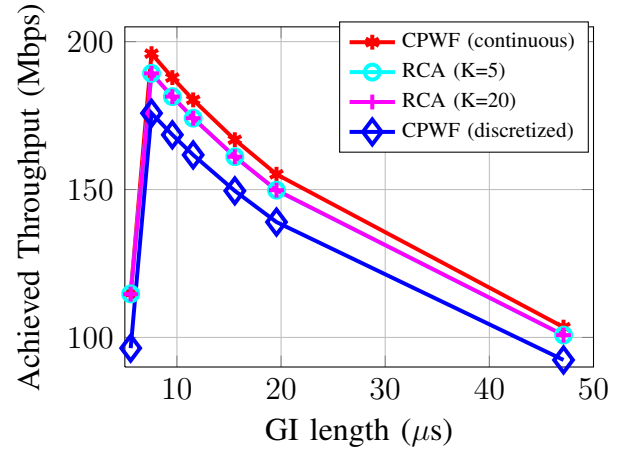


Fig. 12: Throughput with different GI values.

We would choose the GI value corresponding to the maximum capacity. Then, with this GI value, we use the RCA algorithm to determine the bit-loading and power allocation that maximize the achievable throughput.

The cumulative distribution function (CDF) of allocated number of bit and of allocated power for 100 channel realizations are plotted in Figures 13 and 14. We can clearly see that transmitting on Class 5 channel requires less power than on Class 2 channel (mean value: 0.13 vs 0.2) while the throughput obtained in Class 5 channel is higher than that of Class 2 channel (mean value: 8.8 vs 6.2 bit).

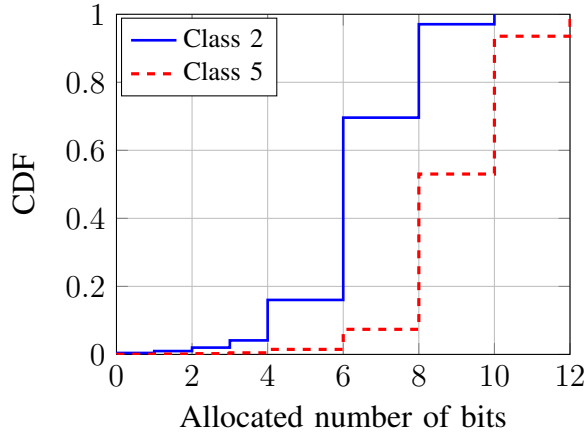


Fig. 13: CDF of the allocated number of bits.

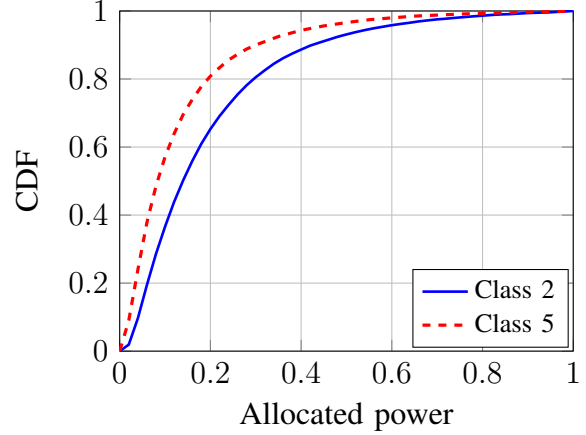


Fig. 14: CDF of the allocated power.

Finally, to adapt the proposed algorithm to the periodically-time varying PLC channels [44], [45], we can re-use the channel adaptation principle described in [44]. In [44], it is assumed that the channel periodically switches among several values. We can use this block-based invariance to apply our proposed algorithm for each channel state. If the frame error rate is high, the channel estimation and the bit/power allocation must be re-operated.

VI. CONCLUSION

In this paper, new robust algorithms for the problem of achievable throughput maximization in PLC systems in presence of interference have been devised. We have developed the greedy algorithms as well as a reduced complexity algorithm. Simulation results have clearly shown that the reduced complexity algorithm is efficient, i.e. the achievable throughput loss is negligible and the complexity is significantly reduced as compared to the greedy solutions. It is also shown that the proposed algorithm is tight with its upper bound of performance and outperforms the MPA and CPWF algorithm. We have also proposed a joint optimization of the GI value and bit/power allocation based on the proposed algorithm. Finally, as the reduced complexity algorithm is based on the greedy principle, it can be also exploited for the margin-adaptive problem with some modifications in the initialization of bit allocation vector. Therefore, it is a good candidate to solve resource management problems for single-user Windowed-OFDM systems in the presence of significant interference.

APPENDIX

INTERFERENCE CALCULATION IN PLC SYSTEMS

In this section, we derive ISI and ICI formula in PLC systems. In other words, we carry out the value of $W(a, b)$, $\forall a, b \in [1, L]$. In this appendix, subcarrier m denotes the m -th available subcarrier. Under a given spectral mask constraint, only a part of available subcarriers is used. According to [11], in absence of noise, the demodulated sample on the m_0 -th subcarrier and n_0 -th OFDM symbol is

$$y(m_0, n_0) = \sum_{m=0}^{M-1} \sum_{n=-\infty}^{+\infty} c_{m,n} \sum_{l=0}^{P-1} h_l e^{-j2\pi m F_0 \tau_l} \underbrace{\frac{1}{T_0} \int_{-\infty}^{+\infty} g(t - nT - \tau_l) f(t - n_0 T) e^{j2\pi(m-m_0)F_0 t} dt}_{I_g(m-m_0, n, n_0, \tau_l)} \quad (35)$$

where

- $c_{m,n}$: Complex QAM, 8-PSK or BPSK symbol located at m -th subcarrier of the n -th OFDM symbol;
- F_0 : frequency separation between adjacent carriers;
- $T_0 = \frac{1}{F_0}$: FFT window period;
- RI : Roll-off interval of the filter at transmitter (utilized in Windowed-OFDM), in the conventional OFDM $RI = 0$;
- GI : Guard interval ($GI > RI$);
- $T = T_0 + GI$: OFDM symbol period;
- $g(t), f(t)$: filter responses at transmitter (length of $T + RI$) and receiver (length of T_0);
- $h(t) = \sum_{l=0}^{P-1} h_l \delta(t - \tau_l)$: Multi-path channel impulse response;

Firstly, the calculation of $I_g(m - m_0, n, n_0, \tau_l)$ is given according to the value of τ_l . There are two cases:

- $\tau_l < \mathbf{GI} - \mathbf{RI}$: The filters at the transmitter $g(t - nT)$ and at the receiver $f(t - n_0 T)$ as well as their relative position are illustrated in Figure 15. In this case, we obtain

$$I_g(m - m_0, n, n_0, \tau_l) = \frac{1}{T_0} \delta_{n,n_0} \int_{GI}^{GI+T_0} e^{j2\pi(m-m_0)F_0(u+n_0 T)} du = \delta_{n,n_0} \delta_{m,m_0} \quad (36)$$

where we used that $T_0 = F_0^{-1}$ and $\delta_{u,v} = 1$ if $u = v$ and null anywhere else.

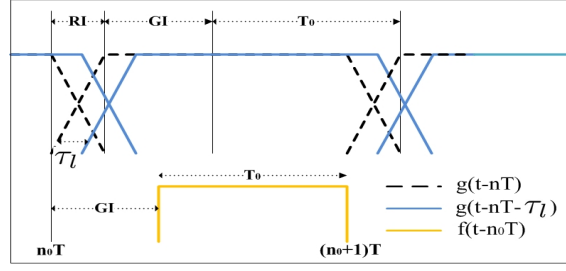


Fig. 15: Relative position of $g(t - nT - \tau_l)$ and $f(t - n_0T)$ in the case of $\tau_l < GI - RI$.

- $GI - RI < \tau_l < T$: Figure 16 illustrates the relative position between both filter responses. By observing Figure 16, we deduce that the term $I_g(m - m_0, n, n_0, \tau_l)$ is not null if and only if $n = n_0$ or $n = n_0 - 1$.

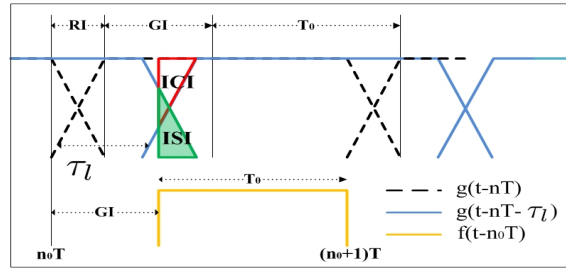


Fig. 16: Relative position of $g(t - nT - \tau_l)$ and $f(t - n_0T)$ in the case of $\tau_l > GI - RI$.

If $n = n_0$:

$$\begin{aligned}
 I_g(m - m_0, n, n_0, \tau_l) &= \frac{1}{T_0} \int_{GI}^T g(u - \tau_l) f(u) e^{j2\pi(m - m_0)F_0(u + n_0T)} du \\
 &= \underbrace{e^{j2\pi(m - m_0)F_0n_0T}}_{C(m - m_0, n_0)} \frac{1}{T_0} \int_{GI}^T g(u - \tau_l) e^{j2\pi(m - m_0)F_0u} du \\
 &= C(m - m_0, n_0) \left[\frac{1}{T_0} \int_{GI}^T e^{j2\pi(m - m_0)F_0u} du \right. \\
 &\quad \left. + \underbrace{\frac{1}{T_0} \int_{GI}^{\tau_l + RI} (g(u - \tau_l) - 1) e^{j2\pi(m - m_0)F_0u} du}_{-G(m - m_0, \tau_l)} \right] \\
 &= C(m - m_0, n_0) \delta_{m, m_0} - A_g(m - m_0, n_0, \tau_l)
 \end{aligned} \tag{37}$$

where $A_g(m - m_0, n_0, \tau_l) = C(m - m_0, n_0)G(m - m_0, \tau_l)$.

If $n = n_0 - 1$: With the same calculation and since $g(u + T) = 1 - g(u)$, $\forall u \in [0, RI]$ we obtain

$$\begin{aligned} I_g(m - m_0, n, n_0, \tau_l) &= \frac{1}{T_0} C(m - m_0, n_0) \int_{GI}^{\tau_l + RI} g(u + T - \tau_l) e^{j2\pi(m - m_0)F_0 u} du \\ &= \frac{1}{T_0} C(m - m_0, n_0) \int_{GI}^{\tau_l + RI} (1 - g(u - \tau_l)) e^{j2\pi(m - m_0)F_0 u} du \\ &= A_g(m - m_0, n_0, \tau_l) \end{aligned} \quad (38)$$

The channel impulse response $h(t) = \sum_{l=0}^{P-1} h_l \delta(t - \tau_l)$ where $\tau_l < \tau_{l+1}$ and $\tau_{IN-1} \leq GI - RI < \tau_{IN}$ can be rewritten as

$$h(t) = \sum_{l=0}^{IN-1} h_l \delta(t - \tau_l) + \sum_{l=IN}^{P-1} h_l \delta(t - \tau_l) \quad (39)$$

Replacing (39) into (35) and taking into account (36), (37) and (38), the analytic formula of $y(m_0, n_0)$ becomes

$$\begin{aligned} y(m_0, n_0) &= \sum_{m=0}^{M-1} \sum_{n=-\infty}^{+\infty} c_{m,n} \sum_{l=0}^{IN-1} h_l e^{-j2\pi m F_0 \tau_l} \delta_{n,n_0} \delta_{m,m_0} \\ &+ \sum_{m=0}^{M-1} \sum_{n=-\infty}^{+\infty} c_{m,n} \sum_{l=IN}^{P-1} h_l e^{-j2\pi m F_0 \tau_l} \{ \delta_{n,n_0} [\delta_{m,m_0} - A_g(m - m_0, n, \tau_l)] + \delta_{n,n_0+1} A_g(m - m_0, n_0, \tau_l) \} \\ &= c_{m_0, n_0} \underbrace{\left(H(m_0 F_0) - \sum_{l=IN}^{P-1} h_l e^{-j2\pi m F_0 \tau_l} A_g(0, n_0, \tau_l) \right)}_{\alpha(m_0)} \\ &- \underbrace{\sum_{m=0, m \neq m_0}^{M-1} c_{m, n_0} \sum_{l=IN}^{P-1} h_l e^{-j2\pi m F_0 \tau_l} A_g(m - m_0, n_0, \tau_l)}_{ICI(m_0, n_0)} \\ &+ \underbrace{\sum_{m=0}^{M-1} c_{m, n_0-1} \sum_{l=IN}^{P-1} h_l e^{-j2\pi m F_0 \tau_l} A_g(m - m_0, n_0, \tau_l)}_{ISI(m_0, n_0)} \end{aligned}$$

In practical PLC systems, c_m is i.i.d $\forall m \in [0, M/2 - 1]$ and $c_m = c_{M-m}^*$, $c_0 = c_{M/2} = 0$. Furthermore, we assume that channel is block-based invariant. Then the values of $W(m_0, m)$, $\forall m, m_0 \in A^{use}$ can be approximated as

$$W(m_0, m) \approx \begin{cases} 2 \left(\mathcal{H}_g(m_0, m) + \mathcal{H}_g(m_0, M - m) \right)^2, & m \neq m_0 \\ \left(\mathcal{H}_g(m_0, m_0) + \mathcal{H}_g(m_0, M - m_0) \right)^2, & m = m_0 \end{cases} \quad (40)$$

where $\mathcal{H}(m_0, m) = \left| \sum_{l=IN}^{P-1} h_l e^{-j2\pi m F_0 \tau_l} G(m - m_0, \tau_l) \right|$.

Because $P(m) = 0, \forall m \notin A^{use}$, then the interference power on subcarrier $m_0 \in A^{use}$ can be re-written as

$$P_I(m_0) = \sum_{m \in A^{use}} W(m_0, m) P(m) \quad (41)$$

Finally, the value of $W(a, b), \forall a, b \in [1, L]$ is defined as $W(a, b) = W(m_0, m)$ where $m_0 = A^{use}(a), m = A^{use}(b)$ and $W(m_0, m)$ is calculated as in Eq. (40).

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